IEEE Xplore ©
RELEASE 2.1

Welcome United States Patent and Trademark Office

:☐:Search Results

BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for "(('integrated circuit' and simulat* and 'state space')<in>metadata)"   ✉e-mail
Your search matched **22** of **1222090** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Publication year** in **Descending** order.

» **Search Options**

View Session History

New Search

» **Key**

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(('integrated circuit' and simulat* and 'state space')<in>metadata)   [»]

☐ Check to search only within this results set

Display Format: ⊙ Citation   ○ Citation & Abstract

Select   Article Information

☐   1. **Time-domain simulation of sampled weakly nonlinear systems using ana integration and orthogonal polynomial series [mixed-signal IC application**
Martens, E.; Gielen, G.;
Design, Automation and Test in Europe, 2005. Proceedings
2005 Page(s):120 - 125 Vol. 1
Digital Object Identifier 10.1109/DATE.2005.311

AbstractPlus | Full Text: PDF(168 KB)   IEEE CNF

☐   2. **Design and analysis of power-CMOS-gate-based switched-capacitor boo inverter**
Yuen-Haw Chang;
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circu Fundamental Theory and Applications, IEEE Transactions on]
Volume 51, Issue 10, Oct. 2004 Page(s):1998 - 2016
Digital Object Identifier 10.1109/TCSI.2004.835681

AbstractPlus | References | Full Text: PDF(1128 KB)   IEEE JNL

☐   3. **Passive reduction algorithm for RLC interconnect circuits with embedde systems (PRESS)**
Saraswat, D.; Achar, R.; Nakhla, M.S.;
Microwave Theory and Techniques, IEEE Transactions on
Volume 52, Issue 9, Part 2, Sept. 2004 Page(s):2215 - 2226
Digital Object Identifier 10.1109/TMTT.2004.834571

AbstractPlus | Full Text: PDF(520 KB)   IEEE JNL

☐   4. **Study of "tanh" ideal and lossy ELIN integrators**
Bozomitu, R.G.; Burdia, D.; Cehan, V.;
Electronics Technology: Meeting the Challenges of Electronics Technology Pr 27th International Spring Seminar on
Volume 2, 13-16 May 2004 Page(s):177 - 183 vol.2

AbstractPlus | Full Text: PDF(269 KB)   IEEE CNF

☐   5. **Cost-efficient block verification for a UMTS up-link chip-rate coprocessor**
Winkelmann, K.; Trylus, H.-J.; Stoffel, D.; Fey, G.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proc
Volume 1, 16-20 Feb. 2004 Page(s):162 - 167 Vol.1
Digital Object Identifier 10.1109/DATE.2004.1268843

AbstractPlus | Full Text: PDF(279 KB)   IEEE CNF

6. **A new nonlinear transient modelling technique for high-speed integrated applications based on state-space dynamic neural network**
Cao, Y.; Ding, R.T.; Zhang, Q.J.;
Microwave Symposium Digest, 2004 IEEE MTT-S International
Volume 3, 6-11 June 2004 Page(s):1553 - 1556 Vol.3
Digital Object Identifier 10.1109/MWSYM.2004.1338875
AbstractPlus | Full Text: PDF(471 KB)   IEEE CNF

7. **Fast and accurate identifying subcircuits using an optimization based tec**
Rubanov, N.;
Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on
Volume 1, 10-11 July 2003 Page(s):69 - 72 vol.1
AbstractPlus | Full Text: PDF(338 KB)   IEEE CNF

8. **Implicit resolution of the Chapman-Kolmogorov equations for sequential application in power estimation**
Freitas, A.T.; Oliveira, A.L.;
Design, Automation and Test in Europe Conference and Exhibition, 2003
2003 Page(s):764 - 769
Digital Object Identifier 10.1109/DATE.2003.1253699
AbstractPlus | Full Text: PDF(367 KB)   IEEE CNF

9. **Efficient simulation of interconnects in high-speed circuits**
Dautbegovic, E.; Condon, M.;
High Frequency Postgraduate Student Colloquium, 2003
8-9 Sept. 2003 Page(s):81 - 84
AbstractPlus | Full Text: PDF(276 KB)   IEEE CNF

10. **Model checking algorithms for analog verification**
Hartong, W.; Hedrich, L.; Barke, E.;
Design Automation Conference, 2002. Proceedings. 39th
10-14 June 2002 Page(s):542 - 547
Digital Object Identifier 10.1109/DAC.2002.1012684
AbstractPlus | Full Text: PDF(728 KB)   IEEE CNF

11. **Guaranteed passive balancing transformations for model order reductior**
Phillips, J.; Daniel, L.; Miguel Silveira, L.;
Design Automation Conference, 2002. Proceedings. 39th
10-14 June 2002 Page(s):52 - 57
Digital Object Identifier 10.1109/DAC.2002.1012593
AbstractPlus | Full Text: PDF(708 KB)   IEEE CNF

12. **Specification-driven test generation for analog circuits**
Variyam, P.N.; Chatterjee, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 10, Oct. 2000 Page(s):1189 - 1201
Digital Object Identifier 10.1109/43.875320
AbstractPlus | References | Full Text: PDF(288 KB)   IEEE JNL

13. **Characterization of a CMOS current-steering DAC using state-space mod**
Andersson, K.A.; Wikner, J.J.;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposiu
Volume 2, 8-11 Aug. 2000 Page(s):668 - 671 vol.2
Digital Object Identifier 10.1109/MWSCAS.2000.952845
AbstractPlus | Full Text: PDF(288 KB)   IEEE CNF

14. **Model order reduction of large circuits using balanced truncation**
Rabiei, P.; Pedram, M.;
Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia
18-21 Jan. 1999 Page(s):237 - 240 vol.1
Digital Object Identifier 10.1109/ASPDAC.1999.760004

AbstractPlus | Full Text: PDF(336 KB)   IEEE CNF

15. **ftd: an exact frequency to time domain conversion for reduced order RL(
models**
Ying Liu; Pileggi, L.T.; Strojwas, A.J.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):469 - 472

AbstractPlus | Full Text: PDF(372 KB)   IEEE CNF

16. **Automatic netlist extraction for measurement-based characterization of (
interconnect**
Corey, S.D.; Yang, A.T.;
Microwave Theory and Techniques, IEEE Transactions on
Volume 45, Issue 10, Part 2, Oct. 1997 Page(s):1934 - 1940
Digital Object Identifier 10.1109/22.641796

AbstractPlus | References | Full Text: PDF(164 KB)   IEEE JNL

17. **An easy approach to formal verification**
Schlipf, T.; Buchner, T.; Fritz, R.; Helms, M.;
ASIC Conference and Exhibit, 1997. Proceedings., Tenth Annual IEEE Interna
7-10 Sept. 1997 Page(s):120 - 124
Digital Object Identifier 10.1109/ASIC.1997.616990

AbstractPlus | Full Text: PDF(516 KB)   IEEE CNF

18. **On the design of micropower active resonators and oscillators using log·
processing**
Ngarmnil, J.; Thanachayanont, A.; Toumazou, C.; Pookaiyaudom, S.;
Electronics, Circuits, and Systems, 1996. ICECS '96., Proceedings of the Thirc
International Conference on
Volume 1, 13-16 Oct. 1996 Page(s):207 - 210 vol.1
Digital Object Identifier 10.1109/ICECS.1996.582779

AbstractPlus | Full Text: PDF(348 KB)   IEEE CNF

19. **Time domain based modeling of lossy coupled transmission lines by apf
transfer functions**
Cyrusian, S.;
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium
Volume 3, 28 April-3 May 1995 Page(s):1840 - 1843 vol.3
Digital Object Identifier 10.1109/ISCAS.1995.523773

AbstractPlus | Full Text: PDF(264 KB)   IEEE CNF

20. **Efficient reduced-order modeling of frequency-dependent coupling induc
associated with 3-D interconnect structures**
Silveira, L.M.; Kamon, M.; White, J.;
European Design and Test Conference, 1995. ED&TC 1995, Proceedings.
6-9 March 1995 Page(s):534 - 538
Digital Object Identifier 10.1109/EDTC.1995.470349

AbstractPlus | Full Text: PDF(380 KB)   IEEE CNF

21. **A guaranteed stable order reduction algorithm for packaging and interco**
Silveira, L.M.; Elfadel, I.M.; White, J.K.;
Electrical Performance of Electronic Packaging, 1993
20-22 Oct. 1993 Page(s):165 - 168
Digital Object Identifier 10.1109/EPEP.1993.394563

AbstractPlus | Full Text: PDF(192 KB)   IEEE CNF

□ **22. Neural algorithms for cell placement in VLSI design**
Caviglia, D.D.; Bisio, G.M.; Curatelli, F.; Giovannacci, L.; Raffo, L.;
Neural Networks, 1989. IJCNN., International Joint Conference on
18-22 June 1989 Page(s):573 - 580 vol.1
Digital Object Identifier 10.1109/IJCNN.1989.118635

AbstractPlus | Full Text: PDF(652 KB)   IEEE CNF